A top layer power supply pattern and a top layer ground pattern are formed. The top layer power supply pattern and the top layer ground pattern are connected to a power supply layer and a ground layer through a plurality of viaholes, respectively. A plurality of capacitors or a plurality of capacitor resistor series circuits are disposed at predetermined intervals between the top layer power supply pattern and the top layer ground pattern.

Roy teaches that power distribution system noise affects computer product timing performance, signal integrity and electromagnetic interference. Between 1 MHz and 1 GHz, the primary means of reducing power distribution noise is with ceramic decoupling capacitors. To achieve a certain target impedance, it is important to characterize the ESR of ceramic decoupling capacitors as they directly determine the number of capacitors required on the board. Another factor which determines the capacitance value of decoupling capacitors is the ESL (inductance) associated with capacitors mounted on a PCB.

Novak teaches that power and ground planes should exhibit low impedance over a wide range of frequencies. Parallel ground and power planes in multiplayer printed-circuit boards exhibit multiple resonances which increase the impedance and also the radiation from the edge of the board. Resistive termination along the board edges reduces the resonance peaks.

In contrast, Applicant teaches an electrical power distribution structure and methods to achieve a target electrical impedance therefor. Independent claim 1 recites, in pertinent part:

> "wherein the mounted inductance L_m of each of the n capacitors is less than or equal to $(0.2 \cdot n \cdot \mu_0 \cdot h)$, and wherein μ_0 is the permeability of free space, and wherein h is a distance between the planar conductors" (Emphasis added).

Similarly, independent claim 8 recites, in pertinent part:

> "determining a separation distance h between the parallel planar conductors required to achieve the target electrical impedance Z_t" (Emphasis added).

Neither Harada, Roy, nor Novak teach or suggest a power distribution structure or method for achieving a target impedance therefor wherein a separation distance between planar conductors is used to determine a mounted inductance (as recited in claim 1) and therefore achieve a target electrical impedance (as recited in claim 8). Applicant can find no teaching or suggestion of this limitation in any of the cited references.

Furthermore, none of the cited references teach or suggest a method for achieving a target electrical impedance as recited in claim 17, which recites, in pertinent part:

> "determining a first required number n_1 of a selected type of discrete electrical capacitor dependent upon an inductance of the electrical power distribution structure L_p and a mounted inductance L_m ... determining a second required number n_2 of the selected type of discrete electrical capacitor dependent upon a distance d_p around an outer perimeter of the electrical power distribution structure ... performing the following if $n_2 \geq n_1$" (Emphasis added)

The cited references, taken singly or in combination, do not teach or suggest this combination of features. Furthermore, Applicant can find no teaching, suggestion, or motivation in either Roy or Novak to modify Harada in order to obtain a method for achieving a target electrical impedance, as recited in claim 17.

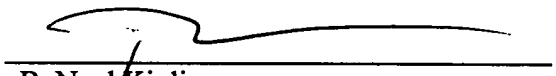
For at least these reasons, Applicant submits that the pending claims patentably distinguish over the cited art. Accordingly, removal of the § 103(a) rejection is respectfully requested.

CONCLUSION

Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Conley, Rose, & Tayon, P.C. Deposit Account No. 501505/5181-62800/BNK.

Respectfully submitted,



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Date: January 10, 2002

MARKED UP COPIES OF THE AMENDED CLAIMS

8. (Amended) A method for achieving a target electrical impedance Z_t in an electrical power distribution structure including a pair of parallel planar conductors separated by a dielectric layer, the method comprising:

determining a separation distance h between the parallel planar conductors required to achieve the target electrical impedance Z_t;

determining a required number n of a selected type of discrete electrical capacitor dependent upon an inductance of the electrical power distribution structure L_p and a mounted inductance L_m of a representative one of the selected type of discrete electrical capacitor when electrically coupled between the planar conductors, wherein $n \geq 2$;

using the target electrical impedance Z_t to determine a required value of mounted resistance $R_{m\text{-}req}$ for the n discrete electrical capacitors;

selecting the required number n of the selected type of discrete electrical capacitor, wherein each of the n capacitors has a mounted resistance R_m substantially equal to the value of required mounted resistance $R_{m\text{-}req}$; and

electrically coupling the n discrete electrical capacitors between the planar conductors.

13. (Amended) The method as recited in claim 8, further comprising:

[determining a separation distance h between the parallel planar conductors required to achieve the target electrical impedance Z_t;]

selecting a thickness t for the dielectric layer such that the thickness t is less than or equal to the required separation distance h;

using thickness t to determine the inductance of the electrical power distribution structure L_p;

selecting the type of discrete electrical capacitor, wherein capacitors of the selected type have at least one substantially identical physical dimension; and

using the at least one substantially identical physical dimension to determine the mounted inductance L_m of the representative one of the selected type of discrete electrical capacitors.